REMARKS

After entry of this amendment, claims 31-60 remain pending. In the present Office Action, claims 1, 4-6, 9-11, 14-16, 19-21, 24-26, and 29-30 were rejected under 35 U.S.C. § 102(b) as being anticipated by Intel 86/88/186/188 User's Manual ("Intel"). Claims 2-3, 7-8, 12-13, 17-18, 22-23, and 27-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Intel in view of Chennupaty et al., U.S. Patent No. 6,014,735 ("Chennupaty"). Applicants respectfully traverse these rejections and request reconsideration. In view of cancellation of claims 1-30, Applicants respectfully submit that the rejections are moot.

New Claims

Applicants respectfully submit that each of new claims 31-60 recite combinations of features not taught or suggested in the cited art. For example, each of claims 31, 35, and 43 recites a combination of features including: "(i) map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field; and (ii) map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field".

Intel teaches the use of a REG field of an instruction and a W bit of an instruction to select a register. Particularly, the W bit specifies whether the operation is a byte or a word operation (Intel, page 1-41, col. 2, lines 5-6 and Figure 1-28). If the W bit specifies a byte operation (W=0), the various encodings of the REG field are mapped to the AL, CL, DL, BL, AH, CH, DH, and BH registers (Intel, page 1-42, Table 1-19). Each of these registers stores a byte. If the W bit specifies a word operation (W=1), the various encodings of the REG field map to various word-sized registers (where a word is 2 bytes).

The Office Action relies on Chennupaty to teach a prefix byte. Chennupaty's prefix byte "uses a prefix code to qualify an existing opcode of an existing instruction" (Chennupaty, col. 1, line 55-56). Chennupaty further teaches selecting an escape code

different from the prefix code and existing opcode (Chennupaty, col. 1, lines 56-59). "The opcode, the escape code, and the prefix code are combined to generate an instruction code which uniquely represents the operation performed by the instruction." (Chennupaty, col. 1, lines 59-62). Thus, Chennupaty teaches prefix codes that are used in combination with opcodes and/or escape codes to identify operations performed by instructions.

Nothing in Chennupaty, Intel, or the alleged combination thereof teaches or suggests "(i) map a value of the register address field to a least significant portion of one of the plurality of registers responsive to the instruction including a prefix field; and (ii) map the value of the register address field to one of a least significant portion or a second least significant portion of one of a subset of the plurality of registers responsive to the instruction excluding the prefix field" as recited in claims 31, 35, and 43. Furthermore, Applicants respectfully submit that Intel and Chennupaty are not properly combinable to form a *prima facie* case of obviousness for claim 31, 35, and 43.

For at least the above stated reasons, Applicants submit that each of claims 31, 35, and 43 are patentable over the cited art. Claims 32-34, being dependent from claim 31, claims 36-38, being dependent from claim 35, and claims 44-50, being dependent from claim 43, are similarly patentable over the cited art for at least the above stated reasons as well. Each of claims 32-34, 36-38, and 44-50 recites an additional combination of features not taught or suggested in the cited art.

Claim 39 recites a combination of features including: "mapping each value of a register address field of an instruction to a least significant portion of a different one of the plurality of registers responsive to an instruction that includes the register address field and includes a prefix field; and mapping each value of the register address field to a least significant portion or a second least significant portion of different ones of a subset of the plurality of registers responsive to the instruction that includes the register address field and excludes the prefix field". The teachings of Intel and Chennupaty, highlighted above, also do not teach or suggest the above highlighted features of claim 39. For at

least the above stated reasons, Applicants submit that claim 39 is are patentable over the cited art. Claims 40-42, being dependent from claim 39, are similarly patentable over the cited art for at least the above stated reasons as well. Each of claims 40-42 recites an additional combination of features not taught or suggested in the cited art.

Claim 51 recites a combination of features including: "the execution core is configured, responsive to an instruction having a register address field, to: (i) utilize a first mapping of values of the register address field to the plurality of registers as a selected mapping responsive to the instruction including a prefix field; and (ii) utilize a second mapping of values of the register address field to the plurality of registers as the selected mapping responsive to the instruction excluding the prefix field, and wherein the execution core is configured to select one of the plurality of registers responsive to a value of the register address field and the selected mapping". The teachings of Intel and Chennupaty, highlighted above, also do not teach or suggest the above highlighted features of claim 51. For at least the above stated reasons, Applicants submit that claim 51 is patentable over the cited art. Claims 52-55, being dependent from claim 51, are similarly patentable over the cited art for at least the above stated reasons as well. Each of claims 52-55 recite additional combinations of features not taught or suggested in the cited art.

Claim 56 recites a combination of features including: "the processor is configured, responsive to an instruction having a register address field, to: (i) utilize a first mapping of values of the register address field to the plurality of registers as a selected mapping responsive to the instruction including a prefix field; and (ii) utilize a second mapping of values of the register address field to the plurality of registers as the selected mapping responsive to the instruction excluding the prefix field, and wherein the processor is configured to select one of the plurality of registers responsive to a value of the register address field and the selected mapping". The teachings of Intel and Chennupaty, highlighted above, also do not teach or suggest the above highlighted features of claim 56. For at least the above stated reasons, Applicants submit that claim 56 is patentable over the cited art. Claims 57-60, being dependent from claim 56, are

similarly patentable over the cited art for at least the above stated reasons as well. Each of claims 57-60 recite additional combinations of features not taught or suggested in the cited art.

Claim Objection

The Office Action objected to claim 7 as being dependent on claim 1, indicating that the dependency should be on claim 6. Applicants have cancelled claim 7. Accordingly, Applicants respectfully submit that the objection is moot.

Previously Submitted Request to Rescind

The Office Action acknowledged the preliminary amendment, and the two information disclosure statements filed in the above-captioned application. However, no mention is made of the Request to Rescind Previous Non-Publication Request. Applicant filed the Request to Rescind on July 25, 2001. Attached hereto as Exhibit A is a copy of the previously-filed Request to Rescind, along with a copy of the date-stamped postcard evidencing receipt of the Request to Rescind in the United States Patent and Trademark Office on July 30, 2001 (along with the preliminary amendment acknowledged in the present Office Action). Applicant respectfully requests acknowledgement of the Request to Rescind in the next action.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-66100/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☒ Other: Exhibit A: Previously filed Request to Rescind and copy of date-stamped post card.

Respectfully submitted,

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